CLAIMS

1. (Currently Amended) A system for keeping time in a clock domain, comprising:

a free-running clock domain having:

a first latch coupled to ~~the~~ an output of ~~the~~ a free-running clock;

an inverter coupled to ~~the~~ an output of the first latch; and

a core mesh-clock domain having:

at least one or more secondary latches coupled to the output of the first latch;

an edge detector coupled to ~~the~~ an output of the secondary latches;

an incrementer coupled to ~~the~~ an output of the edge detector; and

a memory coupled to ~~the~~ an output of the incrementer.

2. (Original) The system of Claim 1, wherein the secondary latches comprise at least two latches coupled in series.

3. (Currently Amended) The system of Claim 1, wherein an output of the memory is coupled to ~~the~~ an input of the incrementer.

4. (Currently Amended) The system of Claim 1, wherein the free-running clock is running at an frequency different than ~~the~~ a core mesh-clock.

5. (Currently Amended) The system of Claim 1, wherein the memory is employable as a storage device for measuring ~~the~~ a passage of time.

6. (Original) The system of Claim 1, wherein the first latch outputs a digital value.

7. (Original) The system of Claim 1, wherein there is a single signal line between the first latch and the one or more secondary latches that crosses between the free-running clock domain and the core mesh-clock domain.

8. (Original) The system of Claim 1, wherein the memory is incrementing at a frequency slower than the free-running clock is incrementing.

9. (Currently Amended) A method of generating a constant time incremental change, comprising:

generating a clock pulse;

generating a voltage level from the clock pulse;

delaying the voltage level through the use of at least one latch;

detecting an edge on the voltage level by an edge detector; ~~and~~

incrementing a value based upon an edge detection; and [[.]]

storing an increment value.

10. (Original) The method of Claim 9, wherein the increment value represents a second clock frequency.

11. (Original) The method of Claim 9, wherein the voltage level is inverted and input into a latch.

12. (Currently Amended) The method of Claim 9, wherein the increment value is stored in a memory.

13. (Currently Amended) The method of Claim 12, wherein ~~the~~ an output of the memory is used by ~~the~~ an incrementer to increment to ~~the~~ a next value.

14. (Currently Amended) The method of Claim 9, wherein the step of delaying the voltage ~~signal~~ level employs a plurality of latches in series.

15. (Currently Amended) The method of Claim 9, wherein ~~the~~ an incrementer employs an n-bit adder.

16. (Currently Amended) The method of Claim 9, wherein ~~the~~ a clock frequency from the clock pulse and ~~the~~ a core mesh-clock frequency from the increment value are not the same frequency.

17. (Currently Amended) The method of Claim 9, wherein an enable signal is conveyed to ~~the~~ a clock for generating the clock pulse.